

REMARKS/ARGUMENTS

The Applicant originally submitted Claims 1-21 in the application. In a previous response, the Applicant amended Claims 1 and 12 and canceled Claim 11 without prejudice or disclaimer. In the present response, the Applicant has amended Claims 1, 12 and 16. No new matter has been added. The Applicant has not added, canceled or amended any other claims.

The Examiner has indicated that dependent Claims 5-6, 8, 10, 16-17 and 19-21 include allowable subject matter. (*See* Examiner's Action, page 3.) As indicated by the below argument, the Applicant believes that all of the pending Claims are allowable. Accordingly, Claims 1-10 and 12-21 are currently pending in the application.

I. Formal Matters and Objections

The Examiner has objected to Claim 16 for including an informality. In response, the Applicant has amended Claim 16 to correct the noted informality. Accordingly, the Applicant respectfully requests the Examiner to withdraw the objection to Claim 16 and allow issuance thereof.

II. Rejection of Claims 1-4, 7, 9, 12-15 and 18 under 35 U.S.C. §102

The Examiner has rejected Claims 1-4, 7, 9, 12-15 and 18 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 6,137,732 to Inaba. The Applicant respectfully disagrees since Inaba does not teach a SRAM device that provides an enhanced low operating voltage V_{ESS} to a SRAM array during at least a portion of an active mode wherein the enhanced low operating

voltage V_{ESS} is at a higher value than a low operating voltage V_{ss} as recited in independent Claims 1 and 12.

Inaba relates to a static semiconductor memory device (SRAM) and a voltage boosting circuit used for the memory device for the purpose of lowering the power supply voltage. (See column 1, lines 7-10.) Inaba discloses a static semiconductor memory device having a ring oscillator 1, a voltage boosting circuit 2 and memory cells 3. The ring oscillator 1 and the voltage boosting circuit 2 cooperate to increase a voltage for the static semiconductor memory device. (See column 7, lines 17-29 and Figure 1.)

The ring oscillator 1 and the voltage boosting circuit 2 of Inaba, however, do not provide an enhanced low operating voltage V_{ESS} for the memory cells 3. Instead, the ring oscillator 1 and the voltage boosting circuit 2 raise the potential of the **word line** of the memory cells 3. (See column 5, line 66 to column 6, line 3; column 7, lines 30-34; and Figure 1.) The Applicant also finds no other teaching in Inaba that discloses providing an enhanced low operating voltage V_{ESS} for the memory cells 3. Thus, Inaba discloses raising the word line voltage to a level required for memory cell writing (see column 6, lines 29-31), but does not address providing an enhanced low operating voltage V_{ESS} for the memory cells 3. Accordingly, Inaba does not teach providing an enhanced low operating voltage V_{ESS} to a SRAM array during at least a portion of an active mode wherein the enhanced low operating voltage V_{ESS} is at a higher value than a low operating voltage V_{ss} as recited in independent Claims 1 and 12.

Thus, Inaba does not teach each and every element of independent Claims 1 and 12 and Claims dependent thereon. Inaba, therefore, does anticipate Claims 1-4, 7, 9, 12-15 and 18.

Accordingly, the Applicant respectfully requests the Examiner to withdraw the §102 rejection with respect to Claims 1-4, 7, 9, 12-15 and 18 and allow issuance thereof.

III. Conclusion

In view of the foregoing amendment and remarks, the Applicant now sees all of the Claims currently pending in this application to be in condition for allowance and therefore earnestly solicits a Notice of Allowance for Claims 1-10 and 12-21.

The Applicant requests the Examiner to telephone the undersigned attorney of record at (972) 480-8800 if such would further or expedite the prosecution of the present application. The Commissioner is hereby authorized to charge any fees, credits or overpayments to Deposit Account 20-0668.

Respectfully submitted,

HITT GAINES, PC



J. Joel Justiss
Registration No. 48,981

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P.O. Box 832570
Richardson, Texas 75083
(972) 480-8800